

EAST - [default.wsp:1]

File View Edit Tools Window Help

Drafts

Pending

Active

- L1: (85) ("hardware description language" or hdl) and ("register transfer level" or rtl) and
- L2: (46) 1 and map\$4 and rout\$4 and (relocat\$4 or optimiz\$4)
- L3: (53) 1 and map\$4 and rout\$4 and (allocat\$3 or relocat\$4 or optimiz\$4)
- L4: (69) partition same netlist
- L5: (3) 3 and 4
- L6: (2) 5 and portion
- L7: (3) 2 and 4
- L8: (2) 7 and portion
- L9: (1) 6 and repeat\$3
- L10: (1) 8 and repeat\$3

Failed

Saved

Favorites

Tagged

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Re
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6192504 B1	20010220	12	Methods and systems for functionally describing a	716/1	716/18 ; 716/3	
2	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6145117 A	20001107	31	Creating optimized physical implementations from	716/18	716/2	
3	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5862149 A	19990119	23	Method of partitioning logic designs for automatic test	714/726	714/738 ; 716/4	

Accessories

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1	<input type="checkbox"/>	<input type="checkbox"/>	US 6192504 B1	20010220	12	Methods and systems for functionally describing a	716/1	716/18 ; 716/3	
2	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6145117 A	20001107	31	Creating optimized physical implementations from	716/18	716/2	

Accessories

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Re
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6192504 B1	20010220	12	Methods and systems for functionally describing a	716/1	716/18 ; 716/3	
2	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6145117 A	20001107	31	Creating optimized physical implementations from	716/18	716/2	
3	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5862149 A	19990119	23	Method of partitioning logic designs for automatic test	714/726	714/738 ; 716/4	

Accessories



- ☐ Drafts
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- ☒ L1: (85) ("hardware description language" or hdl) and ("register transfer level" or rtl) and
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- ☐ Failed
- ☐ Saved
- ☐ Favorites
- ☐ Tagged

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Re
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6192504 B1	20010220	12	Methods and systems for functionally describing a	716/1	716/18 ; 716/3	
2	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6145117 A	20001107	31	Creating optimized physical implementations from	716/18	716/2	



Accessories



⌚ Pending

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L1: (85) ("hardware description language" or hdl) and ("register transfer level" or rtl) and
L2: (46) 1 and map$4 and rout$4 and (relocat$4 or optimiz$4)
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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Re
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6145117 A	20001107	31	Creating optimized physical implementations from	716/18	716/2	



EAST - [default.wsp:1]

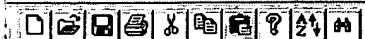
File View Edit Tools Window Help

Drafts
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	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Re
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6145117 A	20001107	31	Creating optimized physical implementations from	716/18	716/2	

Accessories



☒ L12: (5) 9 and split\$4
☒ L13: (11761) duplicat\$4 and
☒ L14: (1) 5696771.pn. and 1
☒ Failed

DBs

USPAT

☒ Plurals

BRS f...

IS&R...

Image

Text

HTML

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comm	Err	Err
1	BRS	L1	133	portion near9 (rtl or netlist)	USPAT	2002/03/11 09:25			0
2	BRS	L2	60	independent and rtl and netlist and map\$4 and optimiz\$6 and test\$4	USPAT	2002/03/11 09:26			0
3	BRS	L3	18	1 and 2	USPAT	2002/03/11 09:26			0
4	BRS	L4	16	plac\$6 and 3	USPAT	2002/03/11 09:27			0
5	BRS	L5	14	4 and allocat\$6	USPAT	2002/03/11 09:27			0
6	BRS	L6	8	5 and (asic or programmable)	USPAT	2002/03/11 09:28			0
7	BRS	L7	450	duplicat\$7 near9 interconnect\$4	USPAT	2002/03/11 09:29			0
8	BRS	L8	0	6 and 7	USPAT	2002/03/11 09:29			0
9	BRS	L9	5	6 and duplicat\$4	USPAT	2002/03/11 09:30			0
10	BRS	L10	5	9 and synthes\$4	USPAT	2002/03/11 09:31			0
11	BRS	L12	5	9 and split\$4	USPAT	2002/03/11 09:32			0
12	BRS	L13	11761	duplicat\$4 and split\$4	USPAT	2002/03/11 09:33			0
13	BRS	L14	1	5696771.pn. and 12	USPAT	2002/03/11 09:34			0



Drafts

Pending

Active

- ☒ L1: (133) portion near9 (rtl or netlist)
- ☒ L2: (60) independent and rtl and netlist an
- ☒ L3: (18) 1 and 2
- ☒ L4: (16) plac\$6 and 3
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- ☒ L7: (450) duplicat\$7 near9 interconnect\$4
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- ☒ L9: (5) 6 and duplicat\$4
- ☒ L10: (5) 9 and synthes\$4
- ☒ L12: (5) 9 and split\$4
- ☒ L13: (11761) duplicat\$4 and split\$4
- ☒ L14: (1) 5696771.pn. and 12

Failed

Search

List

Browse

Queue

Deaf

DBs

USPAT

☒ Abstract

Default operator: OR

☒ Highlight all hit terms titles

5696771.pn. and 12

BRS form

SR form

Image

Text

HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5696771 A	19971209	46	Method and apparatus for performing partial unscan	714/726	716/12; 716/18;



Drafts

Pending

Active

- ☒ L1: (133) portion near9 (rtl or netlist)
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- ☒ L12: (5) 9 and split\$4
- ☒ L13: (11761) duplicat\$4 and split\$4
- ☒ L14: (1) 5696771.pn. and 12

Failed

Search List Browse Queue Clear

DBs USPAT

☒ Plurals☒ Highlight all hit terms initial

9 and split\$4

BRS form IS&R form Image Text HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6067650 A	20000523	46	Method and apparatus for performing partial unscan	714/726	714/724
2	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5903466 A	19990511		Constraint driven insertion of scan logic for	716/18	716/12
3	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5831868 A	19981103		Test ready compiler for design for test synthesis	716/18	
4	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5703789 A	19971230		Test ready compiler for design for test synthesis	716/4	716/5
5	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5696771 A	19971209	46	Method and apparatus for performing partial unscan	714/726	716/12; 716/18;

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☒ Drafts
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☒ Active
☒ L1: (133) portion near9 (rtl or netlist)
☒ L2: (60) independent and rtl and netlist and
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☒ L7: (450) duplicat$7 near9 interconnect$4
☒ L8: (0) 6 and 7
☒ L9: (5) 6 and duplicat$4
☒ L10: (5) 9 and synthes$4
☒ L12: (5) 9 and split$4
☒ L13: (11761) duplicat$4 and split$4
☒ L14: (1) 5696771.pn. and 12

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☒ Plurals

Default operator:
☒ Highlight all hit terms initial

6 and duplicat\$4

☒ BRS form
 ☒ IS&R form
 ☒ Image
 ☒ Text
 ☒ HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6067650 A	20000523	46	Method and apparatus for performing partial unscan	714/726	714/724
2	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5903466 A	19990511		Constraint driven insertion of scan logic for	716/18	716/12
3	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5831868 A	19981103		Test ready compiler for design for test synthesis	716/18	
4	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5703789 A	19971230		Test ready compiler for design for test synthesis	716/4	716/5
5	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5696771 A	19971209	46	Method and apparatus for performing partial unscan	714/726	716/12; 716/18;

EAST - [default1.wsp:1]

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☒ L10: (5) 9 and synthes\$4
☒ L12: (5) 9 and split\$4
☒ L13: (11761) duplicat\$4 and split\$4
☒ L14: (1) 5696771.pn. and 12

Search List Browse Queue Clear

DBs: USPAT ☒ Plurals

Default operator: OR ☒ Highlight all hit terms initial

5 and (asic or programmable)

☒ BRS form ☒ IS&R form ☒ Image ☒ Text ☒ HTML

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6324679 B1	20011127	32	Register transfer level power optimization with	716/18	716/21; 716/3
2	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6141790 A	20001031		Instructions signature and primary input and primary	716/5	703/16; 714/30;
3	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6067650 A	20000523	46	Method and apparatus for performing partial unscan	714/726	714/724
4	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6012155 A	20000104		Method and system for performing automatic	714/727	714/732
5	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5903466 A	19990511		Constraint driven insertion of scan logic for	716/18	716/12
6	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5831868 A	19981103		Test ready compiler for design for test synthesis	716/18	
7	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5703789 A	19971230		Test ready compiler for design for test synthesis	716/4	716/5
8	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5696771 A	19971209	46	Method and apparatus for performing partial unscan	714/726	716/12; 716/18;

Start 9:36 AM

EAST - [default1.wsp:1]

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☒ L2: (60) independent and rtl and netlist an
☒ L3: (18) 1 and 2
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☒ L7: (450) duplicat\$7 near9 interconnect\$4
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☒ L12: (5) 9 and split\$4
☒ L13: (11761) duplicat\$4 and split\$4
☒ L14: (1) 5696771.pn. and 12

Search List Browse Queue Clear
DBs USPAT ☒ Plurals
Default operator: OR ☒ Highlight all hit terms initial
5 and (asic or programmable)

BRS form IS&R form Image Text HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6324679 B1	20011127	32	Register transfer level power optimization with	716/18	716/21; 716/3
2	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6141790 A	20001031	51	Instructions signature and primary input and primary	716/5	703/16; 714/30;
3	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6067650 A	20000523	46	Method and apparatus for performing partial unscan	714/726	714/724
4	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6012155 A	20000104	47	Method and system for performing automatic	714/727	714/732
5	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5903466 A	19990511	37	Constraint driven insertion of scan logic for	716/18	716/12
6	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5831868 A	19981103	35	Test ready compiler for design for test synthesis	716/18	
7	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5703789 A	19971230	36	Test ready compiler for design for test synthesis	716/4	716/5
8	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5696771 A	19971209	46	Method and apparatus for performing partial unscan	714/726	716/12; 716/18;

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EAST - [default1.wsp:1]

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☒ L12: (5) 9 and split\$4
☒ L13: (11761) duplicat\$4 and split\$4
☒ L14: (1) 5696771.pn. and 12

Search List Browse Queue Clear

DBs USPAT ☒ Plurals

Default operator: OR ☒ Highlight all hit terms initial

5 and (asic or programmable)

BRS form ISSR form Image Text HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6324679 B1	20011127	32	Register transfer level power optimization with	716/18	716/21; 716/3
2	<input type="checkbox"/>	<input type="checkbox"/>	US 6141790 A	20001031	51	Instructions signature and primary input and primary	716/5	703/16; 714/30;
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6067650 A	20000523	46	Method and apparatus for performing partial unscan	714/726	714/724
4	<input type="checkbox"/>	<input type="checkbox"/>	US 6012155 A	20000104	47	Method and system for performing automatic	714/727	714/732
5	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5903466 A	19990511	37	Constraint driven insertion of scan logic for	716/18	716/12
6	<input type="checkbox"/>	<input type="checkbox"/>	US 5831868 A	19981103	35	Test ready compiler for design for test synthesis	716/18	
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8	<input type="checkbox"/>	<input type="checkbox"/>	US 5696771 A	19971209	46	Method and apparatus for performing partial unscan	714/726	716/12; 716/18;

Start In... Ex... C... Th... Ap... Do... IE... EA... EA... EA... EA... 9:52 AM



L9: (1) 6 and repeat\$3

L10: (1) 8 and repeat\$3

Failed

	Type	L #	Hits	Search Text	DBs	Time Stamp	Co	E	Err
1	BRS	L1	85	("hardware description language" or hdl) and ("register transfer level" or rtl) and netlist and independent	USPAT	2001/06/21 10:56			0
2	BRS	L2	46	1 and map\$4 and rout\$4 and (relocat\$4 or optimiz\$4)	USPAT	2001/06/21 10:57			0
3	BRS	L3	53	1 and map\$4 and rout\$4 and (allocat\$3 or relocat\$4 or optimiz\$4)	USPAT	2001/06/21 10:58			0
4	BRS	L4	69	partition same netlist	USPAT	2001/06/21 10:59			0
5	BRS	L5	3	3 and 4	USPAT	2001/06/21 11:00			0
6	BRS	L6	2	5 and portion	USPAT	2001/06/21 11:01			0
7	BRS	L7	3	2 and 4	USPAT	2001/06/21 11:01			0
8	BRS	L8	2	7 and portion	USPAT	2001/06/21 11:02			0
9	BRS	L9	1	6 and repeat\$3	USPAT	2001/06/21 11:03			0
10	BRS	L10	1	8 and repeat\$3	USPAT	2001/06/21 11:03			0